ORDRE DES INGÉNIEURS DU QUÉBEC

MAY 2019 SESSION

Open-book examination
Calculators : only authorized models
Duration : 3 hours

14-IF-A3 COMPUTER ARCHITECTURE (100 points)

1. What type of memory is typically used (SRAM or DRAM) to implement a level 1 cache for a very fast processor, and explains the main reasons (10 points)

2. A. How do you call a memory that is divided into memory banks that are accessed sequentially with address 0 at bank 0 and address 1 at bank 1 address 2 at bank 2, etc. It is used to allow sufficient time for the data on a particular bank to be available when accessed providing 0 wait-state accesses for sequential memory addresses. In other words, it divides a main memory in memory banks corresponding to the number of wait states in memory accesses. Then one bank is accessed sequentially one at a time between consecutive accesses such that to allow sufficient time to initiate the following accesses ahead of time so that zero wait state accesses could be done after all banks have been accessed once. It only works for sequential accesses. (10 points)

   B. Where it is typically implemented in a computer (5 points):

3. A. Name 2 main types of snooping protocols (10 points)

   B. Which one is more popular because it typically causes less traffic on the shared bus (5 points)

4. The terms LRU, FIFO, random are used in computer architecture to describe what, and describe what each means (20 points)

5. Is a write buffer important for a data cache and why (10 points)

6. Explain how split transactions work and why it is used (20 points)

7. If a computer has several processors connecting together by a single bus and always executing the same instruction at a given time, is this a SIMD, MISD, or MIMD and give an example of application that could take advantage of such an architecture (10 points)