ORDRE DES INGÉNIEURS DU QUÉBEC

MAY 2017 SESSION

Toute documentation permise
Calculatrices: modèles autorisés seulement
Durée de l'examen: 3 heures

14-IF-A3 Computer Architecture

100 points

1. What type of memory is typically used (SRAM or DRAM) to implement a level 1 and level 2 cache for a very fast processor. Explain the main reasons (10 points)

2. Explains how interleaved memory works and why it is used (20 points)

3. The terms LRU, FIFO, random are used in computer architecture to describe what, and describe what each means (20 point)

4. Is a write buffer important for an instruction cache and why (10 points)

5. Explain how split transactions works and why it is used (20 points)

6. A computer has several processors connecting together by a single bus and operating independently while transferring data to other processors once a while. Is this a SISD, SIMD, MISD, or MIMD and explains why (20 points)