ORDRE DES INGÉNIEURS DU QUÉBEC

NOVEMBER 2017 SESSION

Open-book examination
Calculators : only authorized models
Duration : 3 hours

14-IF-A2 Digital System Design

1) Design a combinational circuit to convert a 4-bit input value, A, B, C and D into a 5-bit output value X, Y, Z, T and U with the following behavior:

   Output X is 1 when none of the input bits is equal to 1, 0 otherwise

   Output Y is 1 when 1 and only 1 of the input bits is equal to 1, 0 otherwise

   Output Z is 1 when 2 and only 2 of the input bits are equal to 1, 0 otherwise

   Output T is 1 when 3 and only 3 of the input bits are equal to 1, 0 otherwise

   Output U is 1 when all the 4 input bits are equal to 1, 0 otherwise

   a) Give the true table for this circuit **(10 points)**
   b) Draw K Maps of the outputs X, Y, Z, T and U **(15 points)**
   c) Design the circuit using elementary gates **(10 points)**

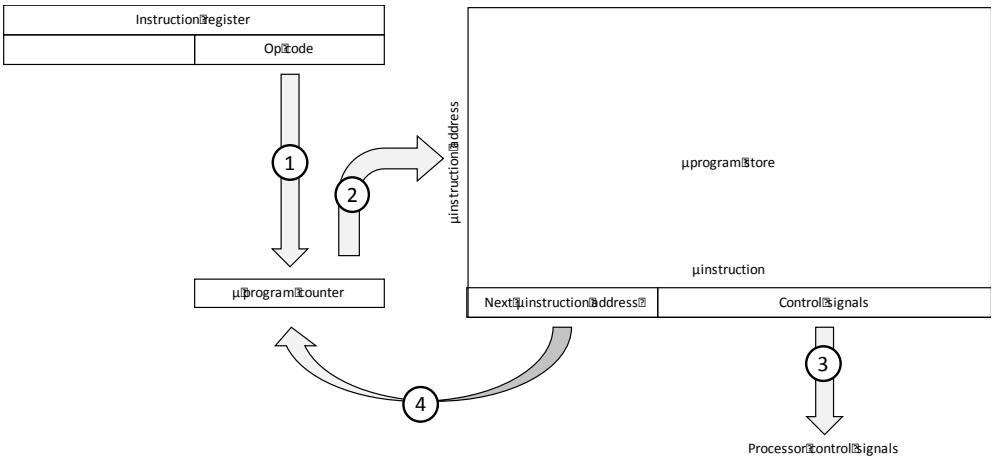
2) Consider a <u>synchronous</u> circuit with one output S and two inputs A and B with a behavior represented by the following transition table:

Actual state	Input A	Input B	New output S	Next state
0	0	X	0	0
0	1	X	1	1
1	1	X	1	1
1	0	1	0	0
1	0	0	1	1

   a) Plot a sample of the time sequence operation of this circuit **(10 points)**
   b) Draw the state diagram of the system **(10 points)**
   c) Design the circuit with D flip-flop(s) **(10 points)**
   d) Describe in English text the behavior of the circuit **(10 points)**

3) Explain the roles of the chip select (CS) and read/write (R\W) signals used to access memory devices or peripheral circuits on a microcomputer. Give an example of a circuit diagram of an interconnection between a memory device and a microprocessor. **(10 points)**

4) A microprogrammable processor with an addressable memory is considered (addressable control store) which contains micro code firmware to execute each of the instructions available to that processor. Each microinstruction comprises two bit fields: one with all the control signals of the processor indicating which ones will be activated by this microinstruction and the other containing the address of the next microinstruction to be executed. The architecture of this part of the processor is reproduced in the following figure:



a) Explain each of the identified steps from 1 to 4 **(10 points)**

b) Is there a limitation associated with step 1 and how do you remedy it? **(5 points)**